

SECRET 44-2460

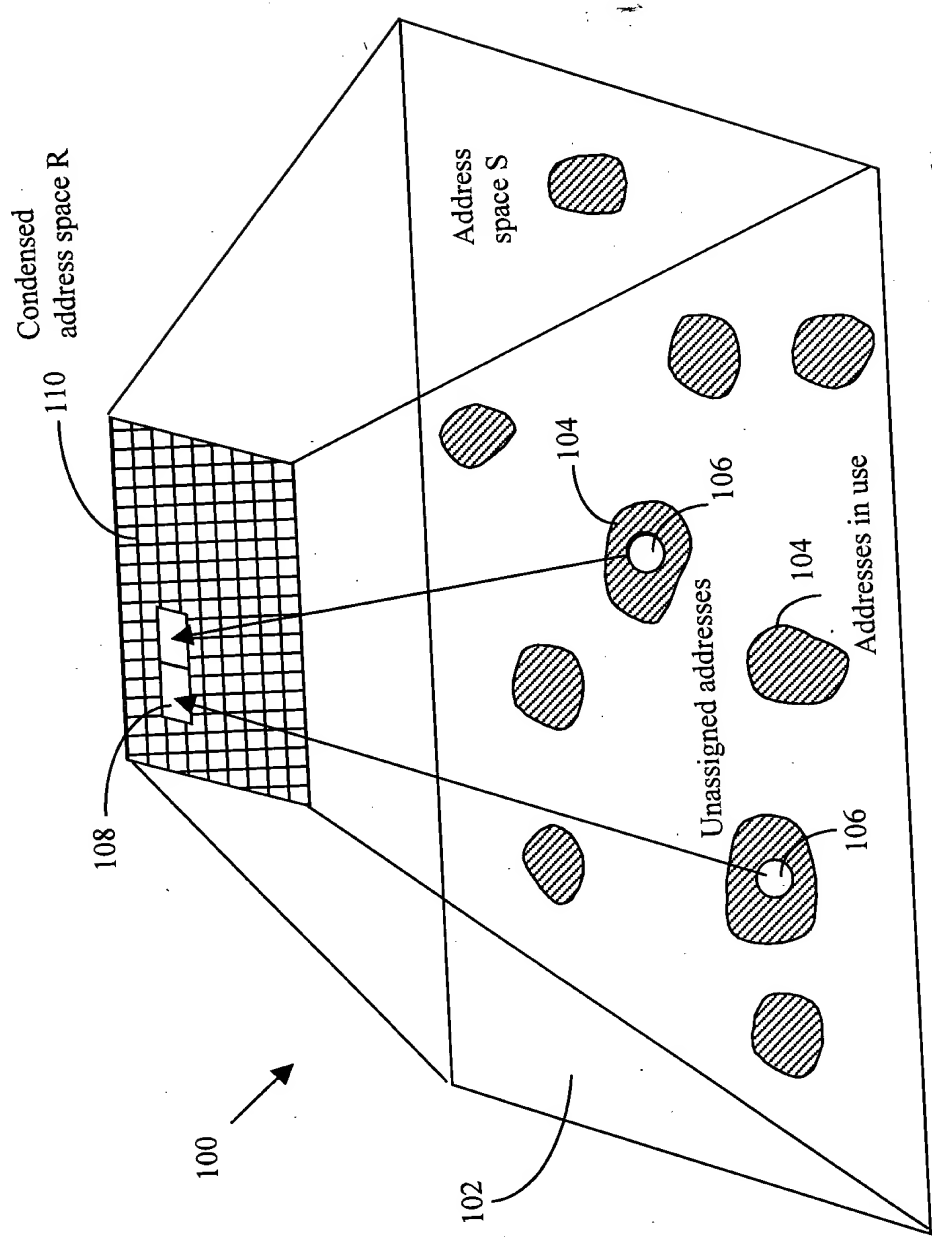
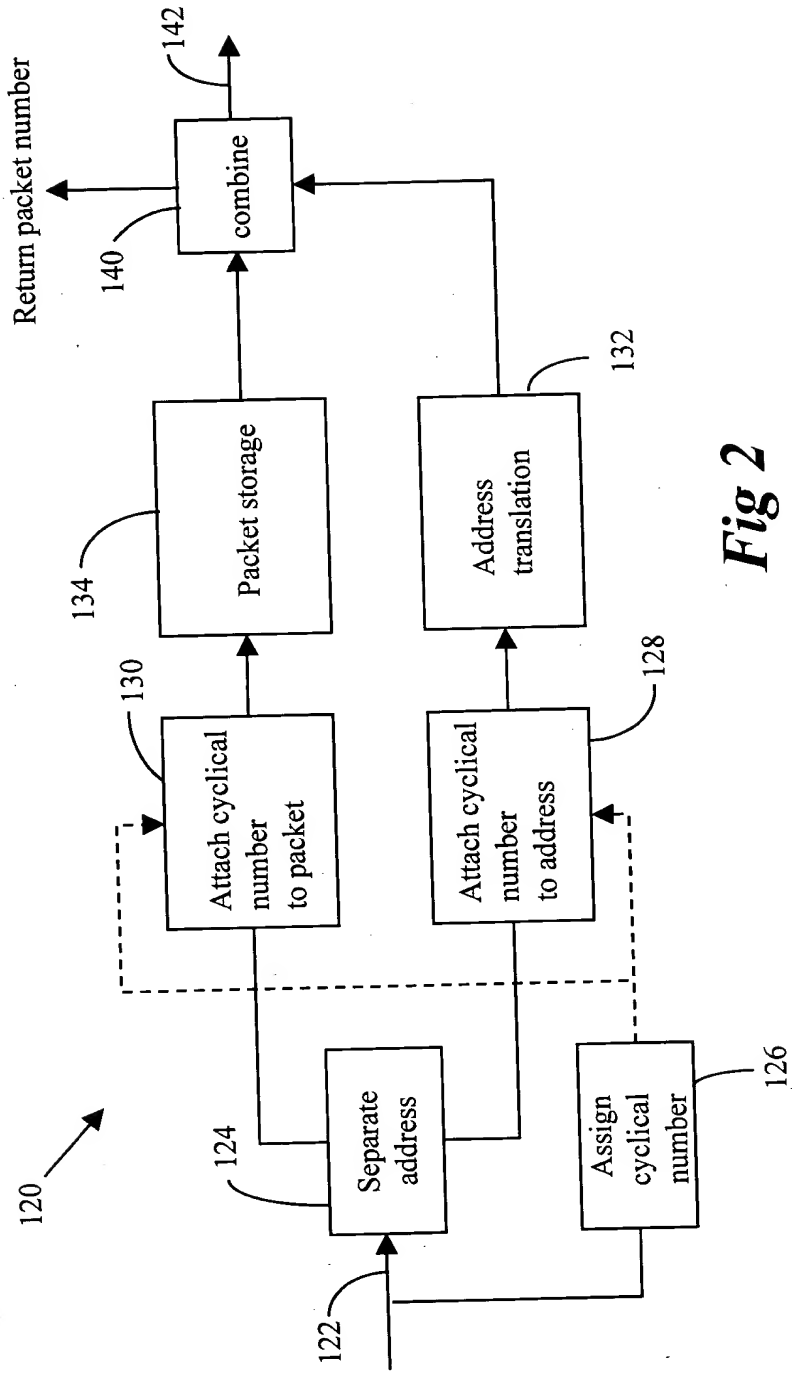
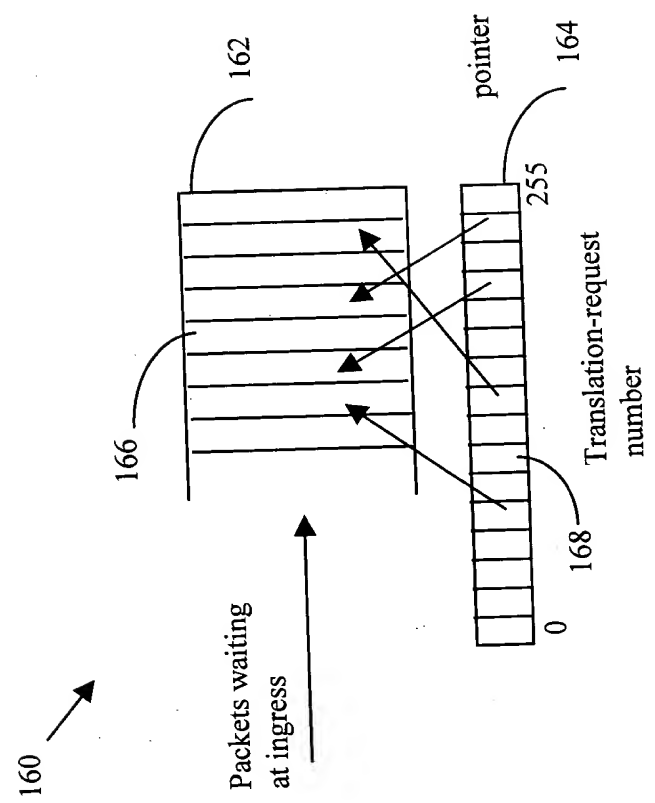


Fig 1

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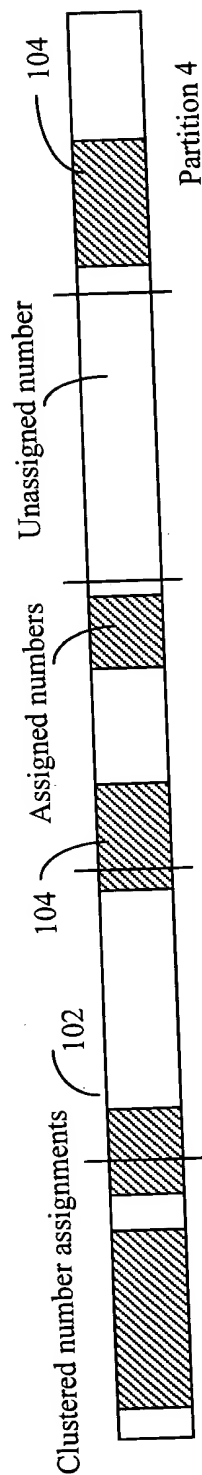
**Fig 2**



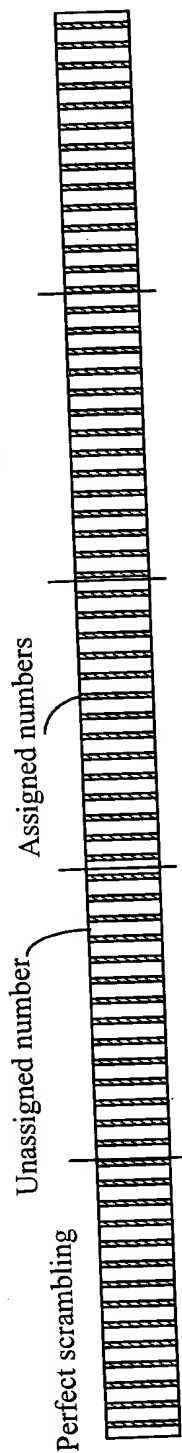
Packet & address are identified by ingress port number and translation request number

Fig 3

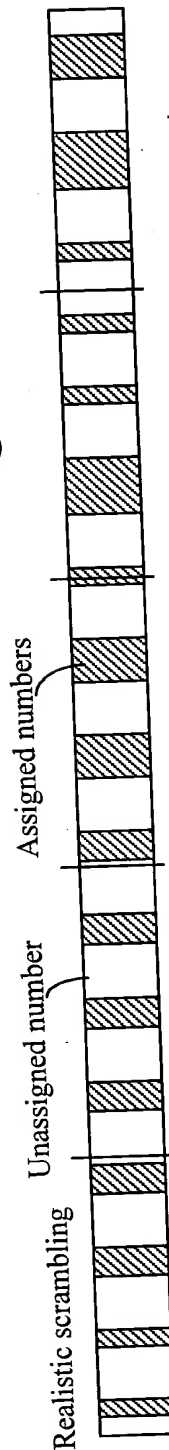
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**Fig 4a**



**Fig 4b**



**Fig 4c**

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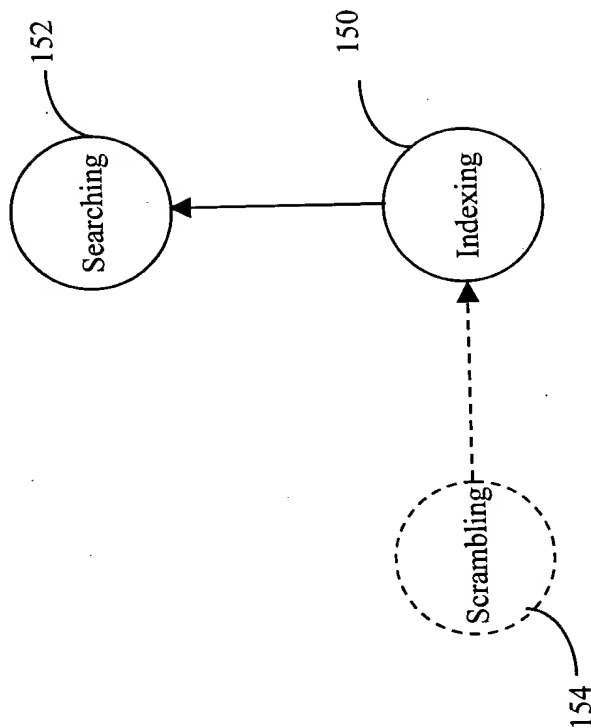


Fig 5

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170

Direct	4	5	6	7	17	18	19	20	21	22	23
Bit-reversed	4	20	12	28	17	9	25	5	21	13	29

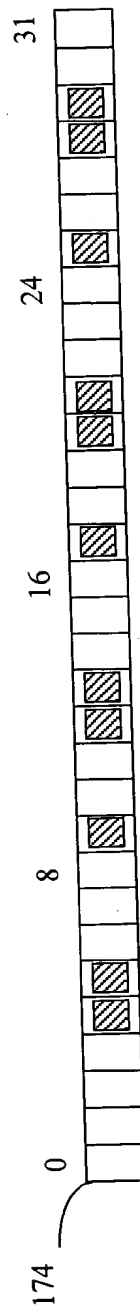
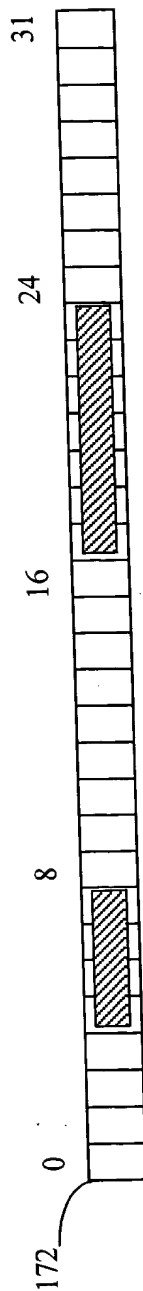


Fig 6

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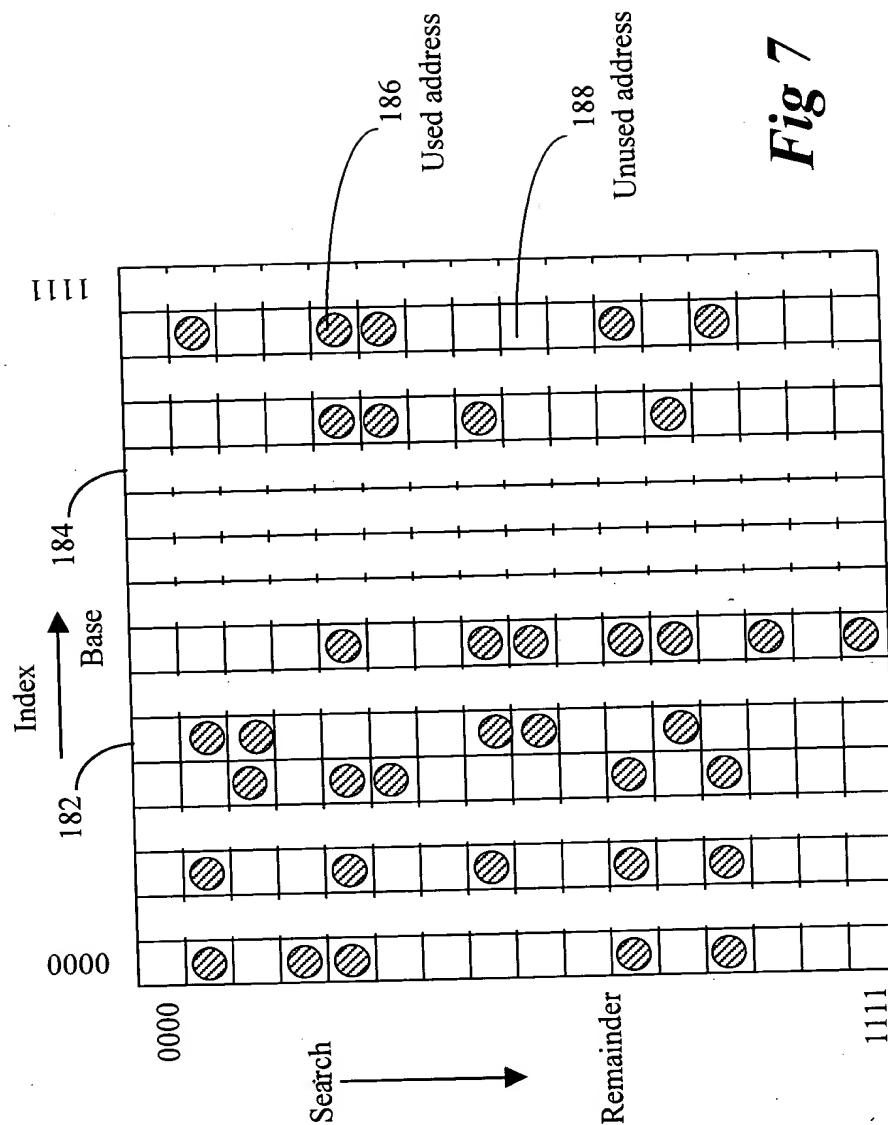


Fig 7

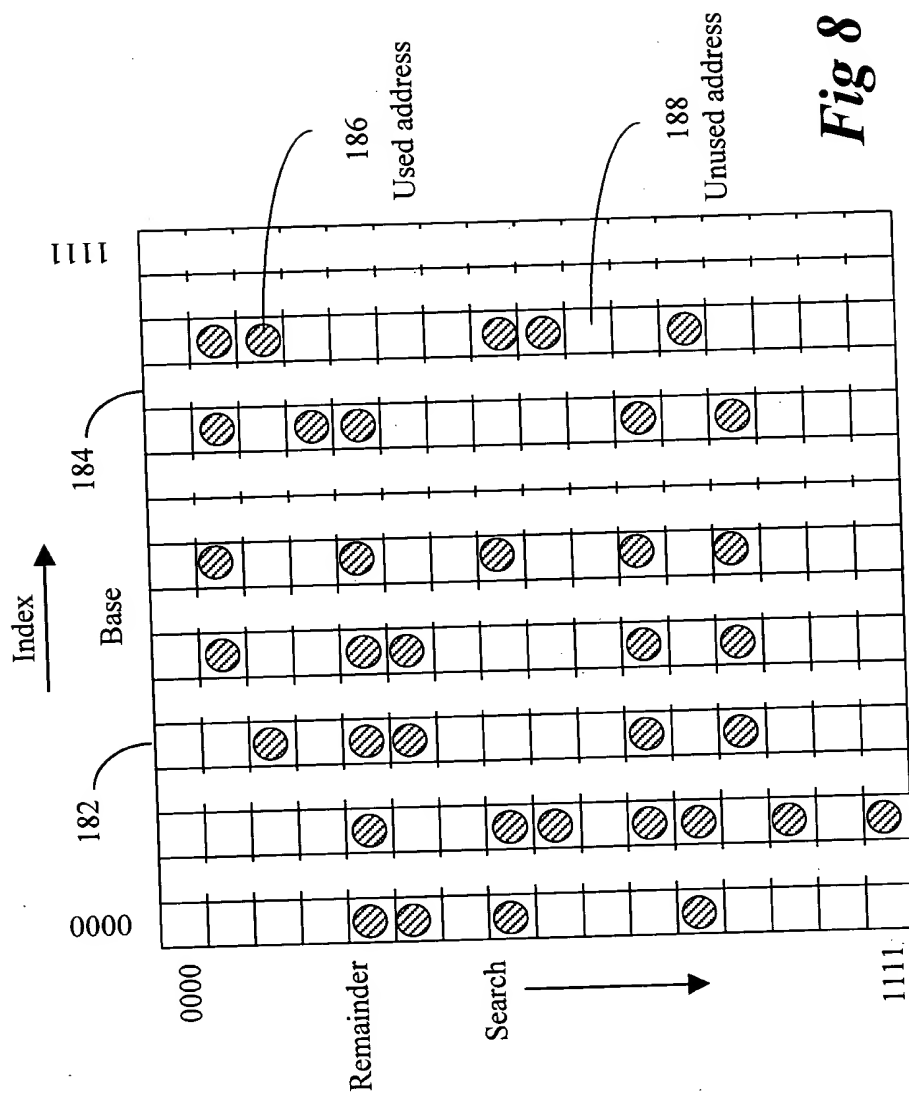
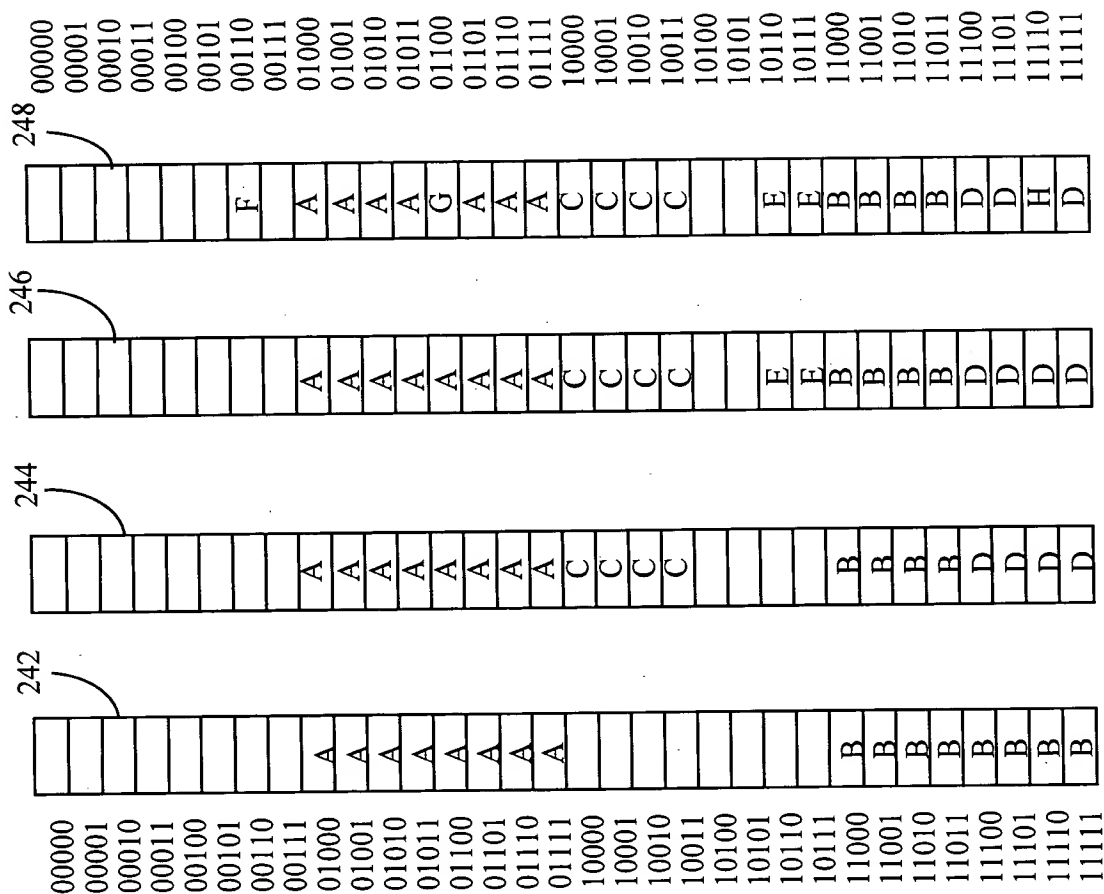


Fig 8



A	01
B	11
C	100
D	111
E	1011
F	00110
G	01100
H	11110

**Fig 9**



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Five digits addresses			
11011	S	00000	A
11000	R	00001	A
10010	Q	00010	H
		00011	H
		00100	E
		00101	E
		00110	E
		00111	E
01110	P	01000	F
0001	H	01001	F
		01010	F
111	G	01011	F
010	F	01100	P
001	E	01101	P
		01110	B
11	D	01111	B
10	C	10000	C
01	B	10001	C
00	A	10010	Q
		10011	C
		10100	C
		10101	C
		10110	C
		10111	C
		11000	R
		11001	D
		11010	D
		11011	S
		11100	G
		11101	G
		11110	G
		11111	G

Fig 10

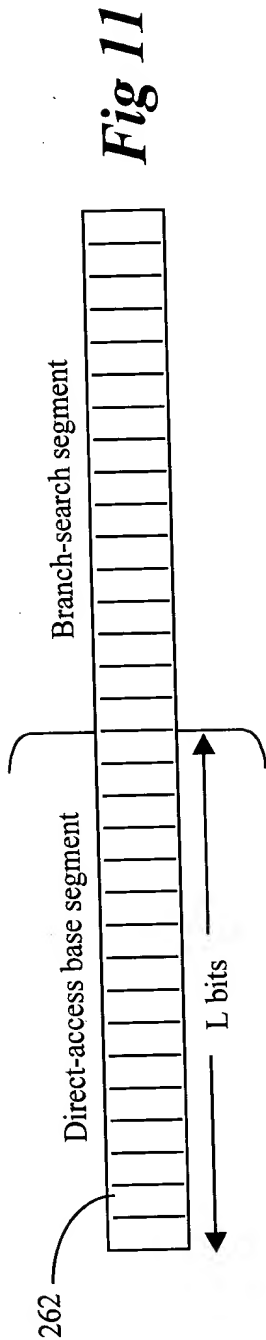


Fig 11

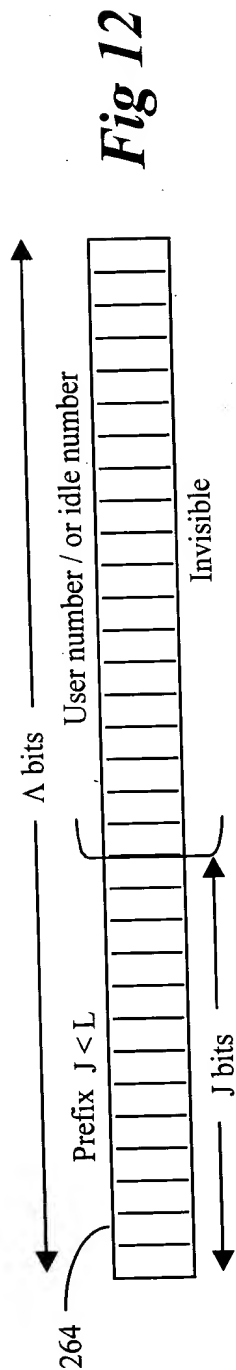


Fig 12

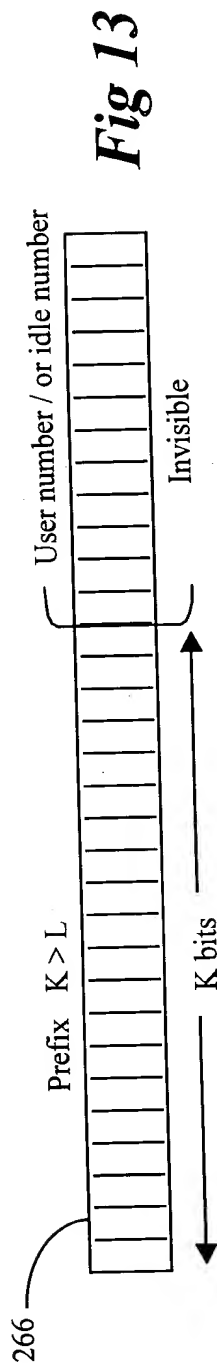
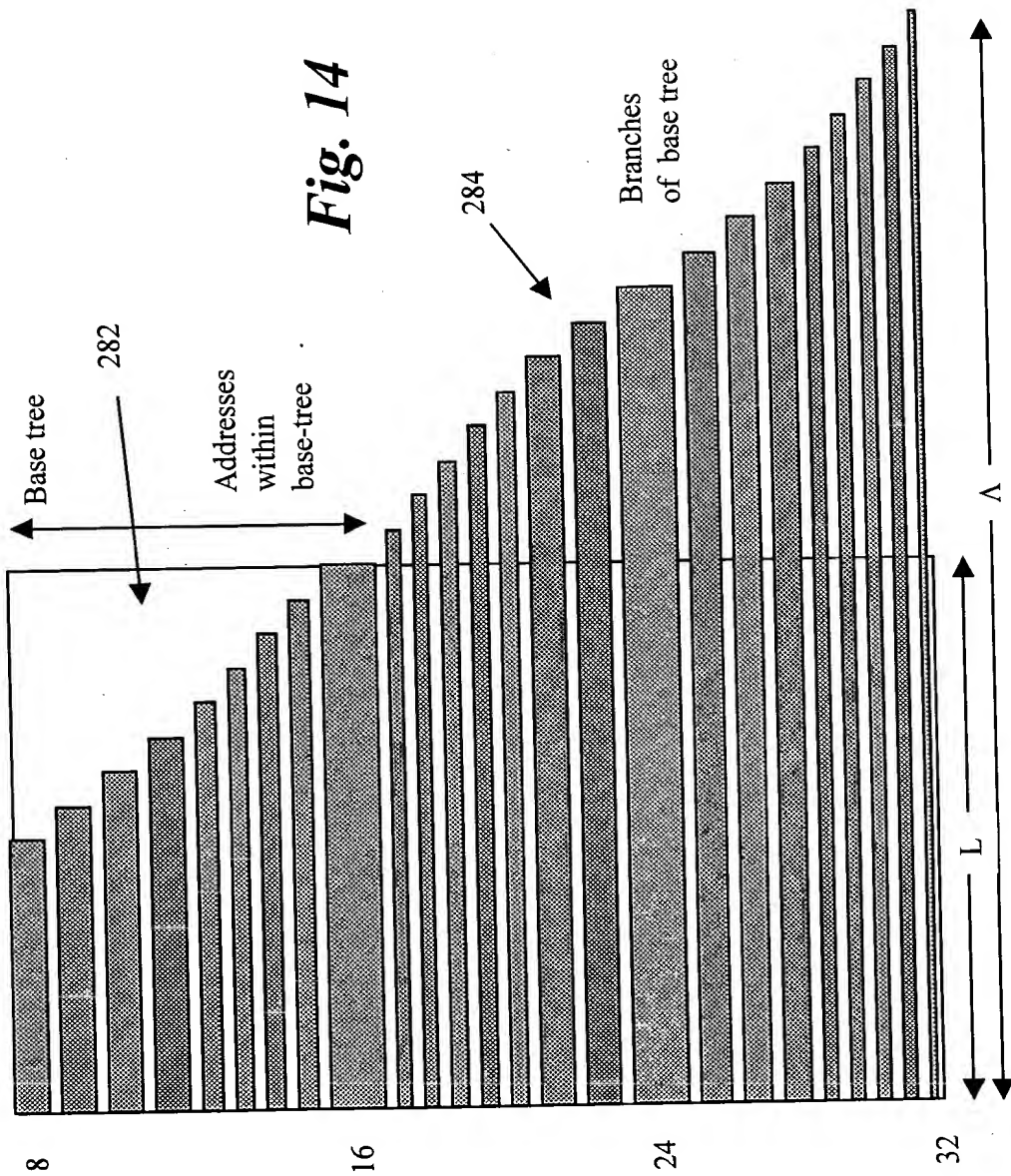
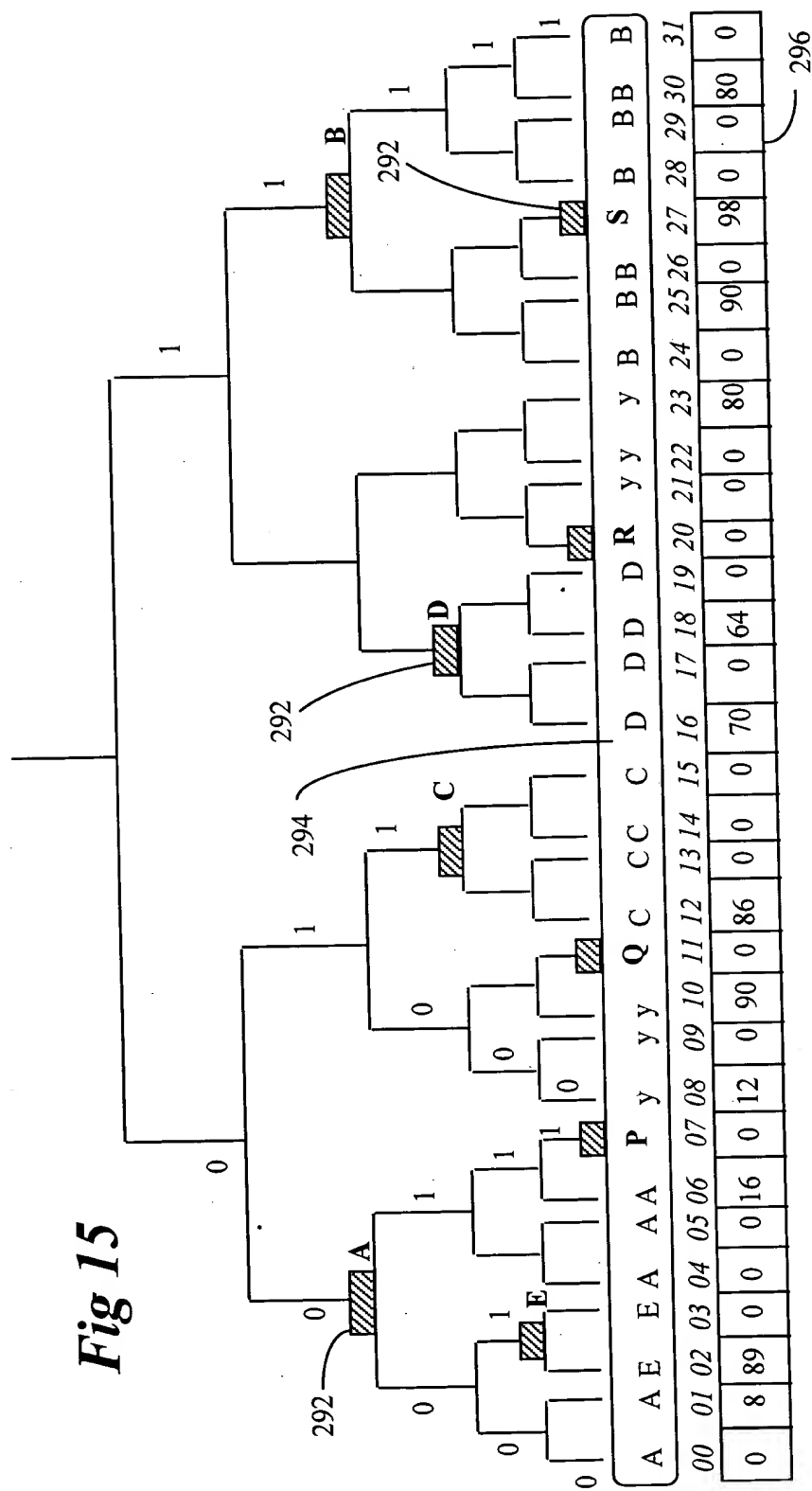


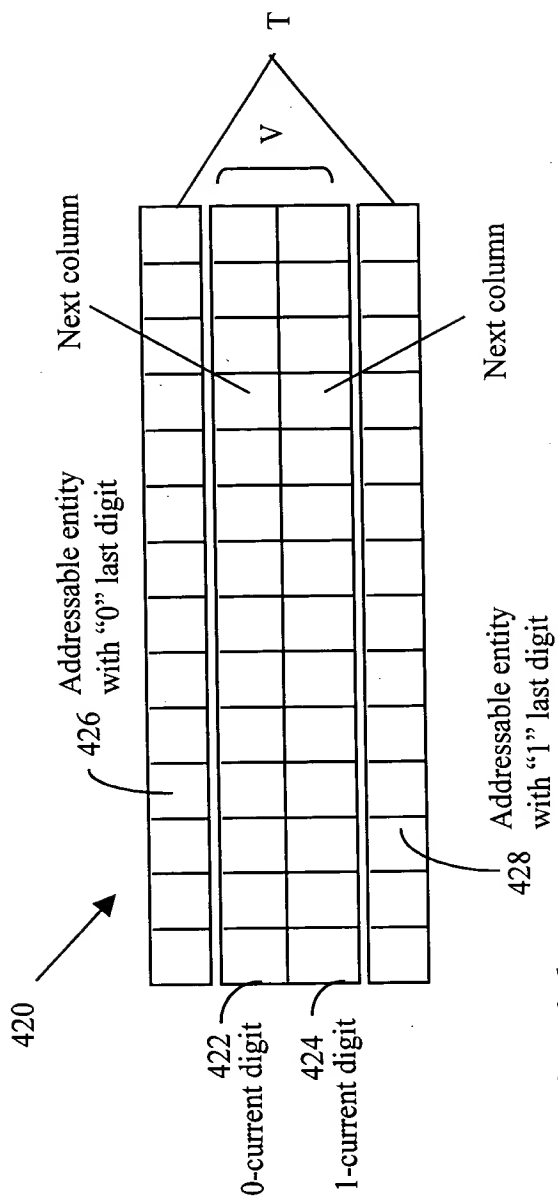
Fig 13



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Fig 15



[illegible]

[illegible]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
									C3													
0							8															
1			7					9														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

[illegible]

				A1	C3	B1	C1	B4	A3			A2
5	21			8		17		19				
11	10	7	14	6	16	9	22	12	13	15	18	20
					B3	B2		A4		D1	C4	C2

**Fig 17**

[illegible]

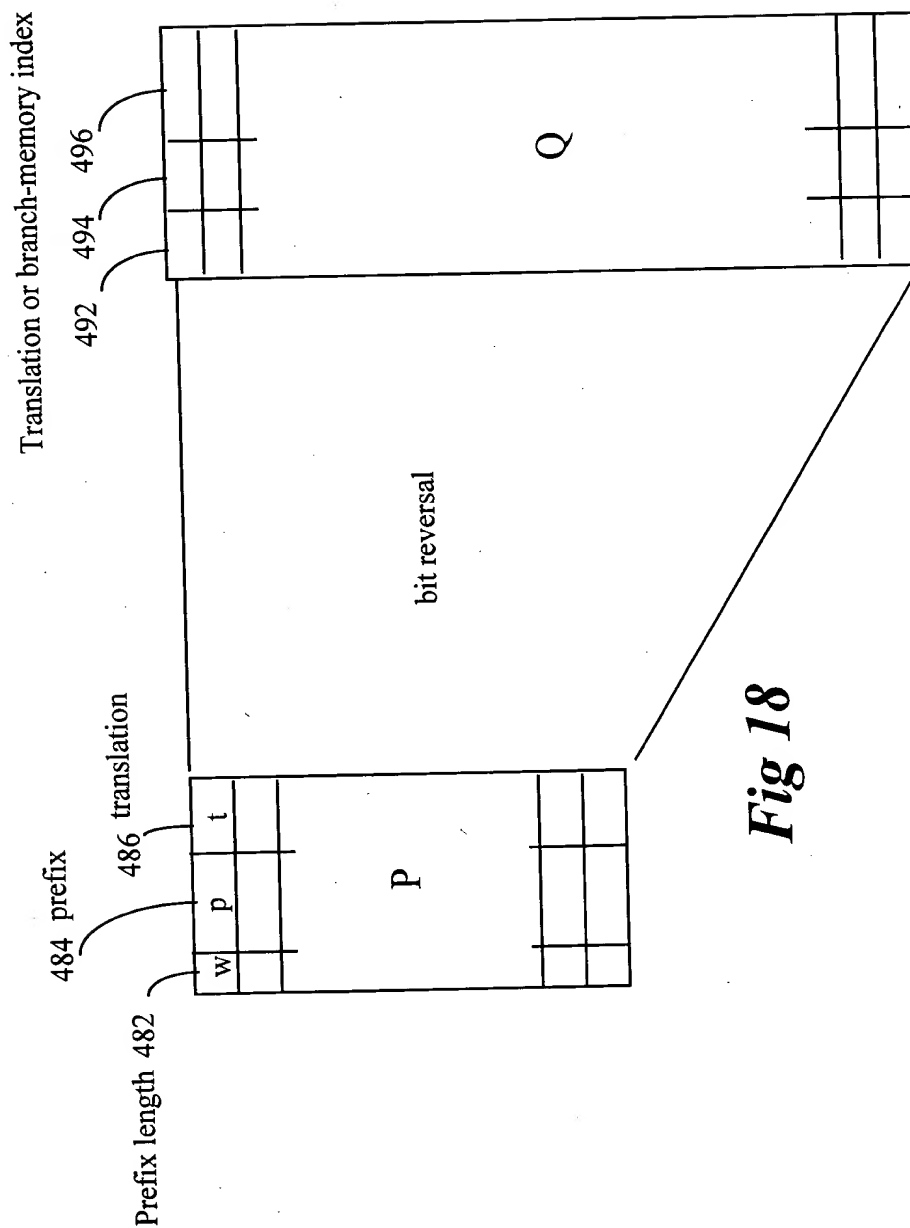


Fig 18



FIG. 19

482	w	p	t	486
2	01		A	
2	10		B	
3	011		C	
3	101		D	
4	1010		E	
5	10010		F	
5	11000		G	
5	10011		H	
5	10100		I	
6	110011		J	
7	1010111		K	
7	1111000		L	
7	0010101		M	
7	0000111		P	
7	1100000		Q	
7	1001000		R	
7	1101010		S	
8	10101111		T	
8	00010000		U	
8	11101111		V	
8	00110000		W	

480

Fig 19

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490				490				490			
492				492				492			
0000	00			0000	00			0000	10	2	P
0001	00			0001	00			0001	10	4	U
0010	00			0010	00			0010	10	1	M
0011	00			0011	00			0011	10	2	W
0100	01	A		0100	01	A		0100	01	A	
0101	01	A		0101	01	A		0101	01	A	
0110	01	A	C	0110	01	C		0110	01	C	
0111	01	A	C	0111	01	C		0111	01	C	
1000	01	B		1000	01	B		1000	01	B	
1001	01	B		1001	10	2	F, H	1001	10	2	F, H, R
1010	01	B	D	1010	10	1	E, I	1010	10	1	E, I, K, T
1011	01	B	D	1011	01	D		1011	01	D	
1100	00			1100	10	3	G, J	1100	10	3	G, J, Q
1101	00			1101	00			1101	10	3	S
1110	00			1110	00			1110	10	1	V
1111	00			1111	00			1111	10	4	L

Fig 20

66E22T-112F460

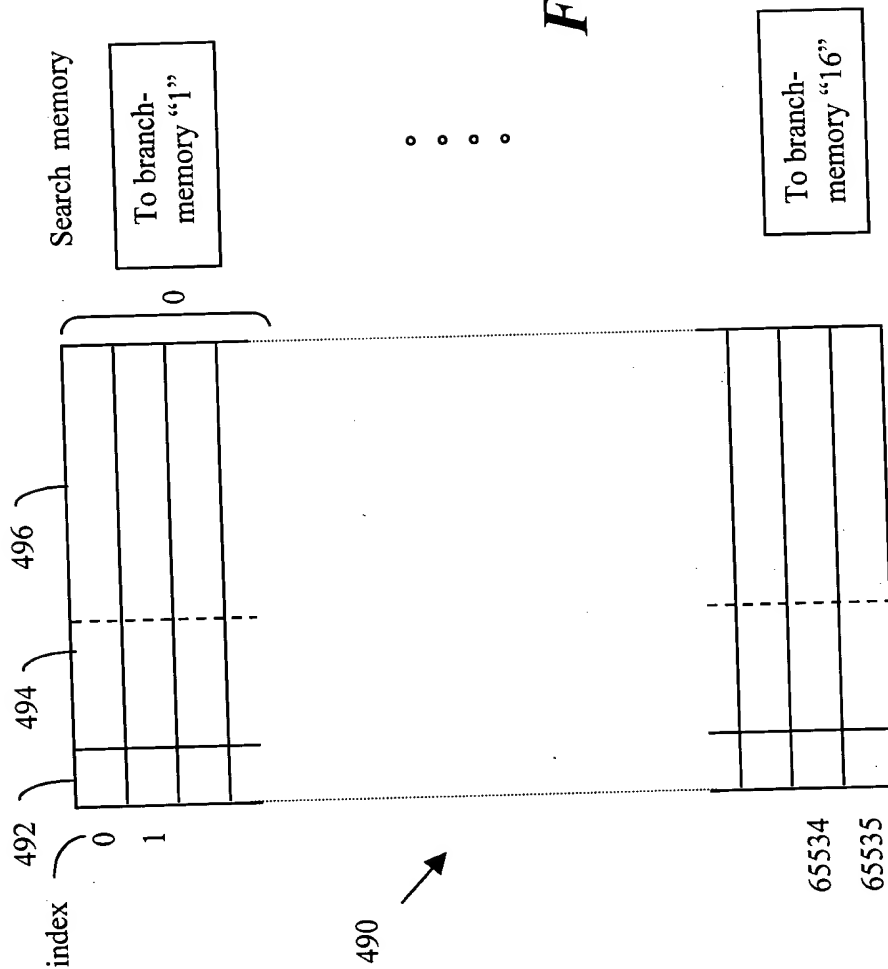


Fig 21

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490 →

	Translation code 492	secondary memory 494	Branch number in secondary memory 496
0	10	1	1
1	10	1	2
2	10	1	3
3	10	1	4
4	01	12	
5	10	2	1
6	10	2	2
7	00	Don't care	
8	10	3	1
9	01	16	
10	10	3	2
11	10	3	3
12	10	4	1
13	10	4	2
14	10	4	3
15	00	Don't care	

00: void  
 01: translation  
 10: pointer to secondary memory

Fig 22

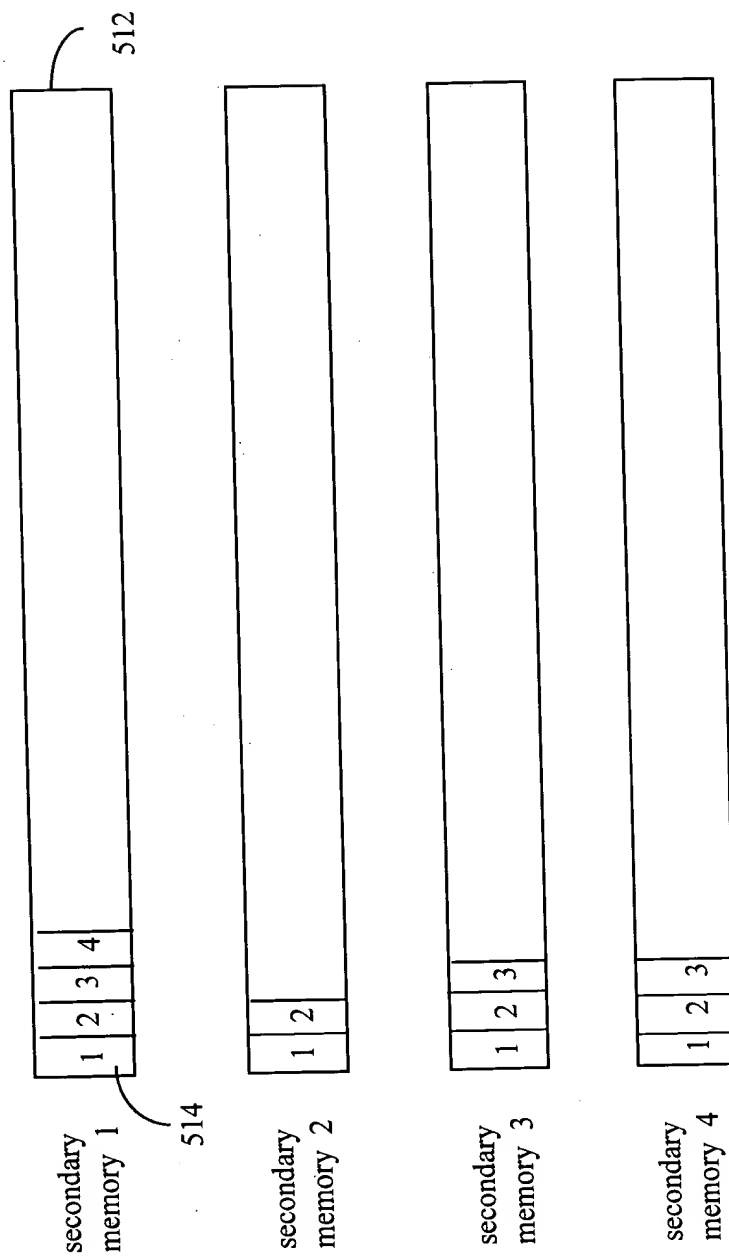
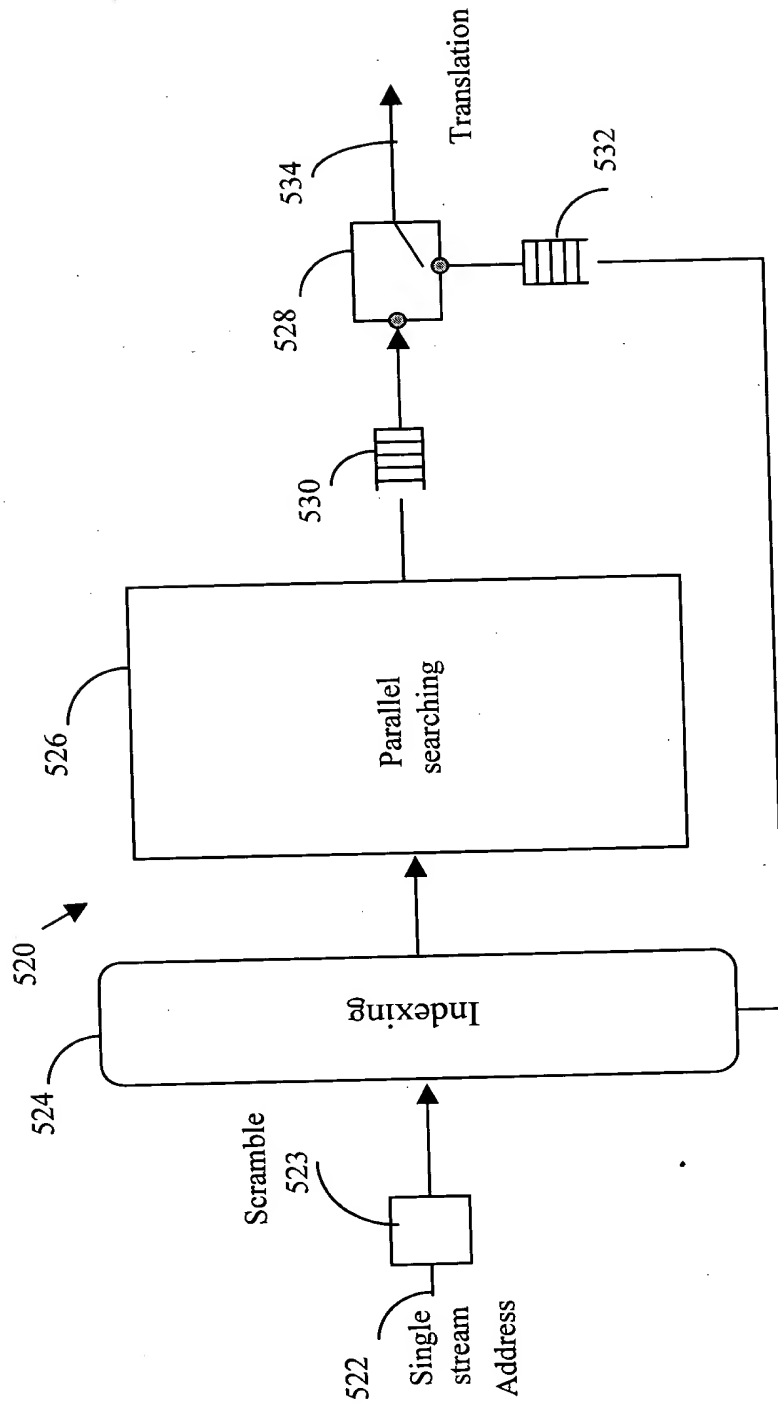


Fig 23

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**Fig 24**

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